Trigger and Data Acquisition electronics for the Geiger-mode avalanche photodiode Cherenkov Telescope Camera of FACT

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Abstract: Within the framework of the FACT project (First G-APD Cherenkov Telescope), we develop and construct a camera based on Geiger-mode avalanche photodiodes (G-APD) for Imaging Atmospheric Cherenkov Telescopes. Such Cherenkov telescopes are the workhorses in ground-based very high energy gamma-ray astronomy. Compared to the currently used photomultiplier tubes, G-APDs promise higher photon detection efficiency, are more robust and operate at a much lower bias voltage. The FACT camera is equipped with 1440 pixels and data acquisition channels. Preamplifiers, data acquisition, trigger electronics and slow control are integrated in the camera. The readout system is based on the DRS4 analogue pipeline chip, operated at a default sampling rate of 2 GHz. Data transfer from the camera to the data acquisition computers is based on standard TCP/IP Ethernet connections. The trigger system uses analogue sums over trigger patches that consist of 9 pixels each, with the possibility to exclude individual pixels from the trigger generation.

Keywords: Geiger-mode avalanche photodiodes (G-APD), DRS4 Domino Ring Sampling Chip, Imaging Atmospheric Cherenkov Telescope (IACT), First G-APD Cherenkov Telescope (FACT), Cherenkov telescope, ground-based gamma-ray astronomy

1 Introduction

So far, all operational Imaging Atmospheric Cherenkov Telescopes (IACTs) use cameras based on photomultiplier tubes (PMTs). Nevertheless, since several years, solid state photodetectors, the so-called G-APDs [1] become available. These G-APDs are auspicious compared to the PMTs used up to now: G-APDs promise a higher photon-detection efficiency, they allow single photon resolution and are insensitive to bright light. Furthermore G-APDs require a much lower bias voltage of about 70 V instead of the kVs required by PMTs, and are mechanically more robust. Aging effects in G-APDs are not known so far and in contrast to PMTs, G-APDs are insensitive to magnetic fields. Although a small-scale prototype of a G-APD based camera has successfully been used to record cosmic ray induced air showers [2], a full-scale camera has not yet shown its performance. Therefore, the conclusive proof that G-APDs are a viable replacement for PMTs in future IACT cameras[1] is still missing. In this proceeding, the trigger and data-acquisition electronics of the FACT Camera, the first full-scale G-APD based IACT camera, is presented.

1. As for the planned Cherenkov Telescope Array [3]

2 General Layout of the FACT Camera

The two main parts of the FACT camera are the sensor compartment with the solid parabolic light concentrators [4, 5] and the G-APDs [1] as well as the electronics compartment with the trigger- and readout electronics.

The FACT camera comprises 1440 pixels and the same number of readout channels. The readout- and trigger electronics is subdivided into four crates containing ten preamplifer- trigger- and digitizer boards each. The preamplifer- trigger unit- and digitizer boards have 36 channels each, resulting in 40 boards of each kind. An overview of the FACT camera electronics is given in the block diagram in figure 1.

In addition to the four crates of trigger- and readout electronics the FACT camera also comprises one trigger master board, two fast signal distribution boards, a slow control board, power converters, water cooling and a lightpulser in the camera shutter for test purpose. A second lightpulser for feedback and calibration purposes (see [6]) is to be placed at the center of the telescope's mirror dish. Beside this lightpulser and the cooling unit, the only component not integrated in the FACT camera is the bias voltage supply (see subsection 2.6).

2.1 Preamplifier

The preamplifier board comprising 36 channels i.e. four trigger patches, performs a current to voltage conversion and an amplification of the signal coming from the G-APD. The amplified signals are then fed to the corresponding data-acquisition board (see subsection 2.3) for digitization. The preamplifier board also performs a patch-wise summation of the nine signals of each trigger patch. After the summation, the trigger threshold provided by the trigger unit (see subsection 2.2) is applied and the resulting comparator signal is then fed to the trigger unit. The preamplifier board carries the trigger unit as a mezzanine board.

2.2 Trigger unit

The trigger unit sets a discriminator threshold to every trigger patch consisting of nine pixels. The discriminator signals from all four patches are collected by the trigger unit and the corresponding rates are monitored (counted) in an on-board FPGA (Field-programmable Gate Array). This F-PGA is also controlling the DAC (digital-to-analogue converter) used to set the discriminator thresholds. The patch-wise trigger signals are fed to an 'n-out-of-4' logic generating a single signal that serves as trigger primitive. This trigger primitive signal is fed to the trigger master board (see subsection 2.4) as well as its rate monitored on board in the same manner as the four discriminator signals. In addition, the trigger unit, together with the preamplifier, provides the possibility to exclude single pixels from a trigger patch. This is forseen do deal with noisy or defective pixels as well as with stars in a trigger patch. The trigger unit features an RS-485 bus to provide a communication link to the trigger master for slow-control purpose such as setting thresholds (i.e. DAC values) and reading out rates. Mechanically, the FTU board is designed as a mezzanine board sitting on the preamplifier board, while the trigger primitive signal is fed to the trigger master by means of a coaxial cable.

2.3 Data-acquisition board

The data-acquisition of the FACT camera is based on the DRS4 [7] analogue pipeline chip designed at the Paul Scherrer Institute in Switzerland. The DRS4 chip is a switched capacitor array with 9 channels and 1024 storage cells per channel. It can be operated at sampling rates from 700 MSPS to 5 GSPS. For FACT, a default sampling rate of 2 GSPS is planned. After the DRS4 chip, an external analogue to digital converter is required, which is, in our case operated with a sampling clock of 25 MHz. The dynamic range (effective number of bits) is 11.5 bits - enough to allow for a single photoelectron resolution assuming a maximum range of about 200 photoelectrons per channel. The DRS4 chip allows the region of interest (ROI) i.e. the number of slices to be read out and subsequently digitized, to be set individually for each channel. Every board features four DRS4 chips and a 100 Mbps Fast Ethernet interface for data readout and slowcontrol purpose. In order to receive the trigger-IDs from the trigger master (see susection 2.4), every board is equipped with a dedicated RS-485 bus. The trigger-ID is sent to the data-acquisition computer together with the data.

2.4 Trigger Master

The FACT Trigger master collects the 40 trigger primitives from the trigger units to generate the trigger- and the timemarker signal. Furthermore it generates the reference clock for the DRS4 chips (see subsection 2.3) and the resets signals, as well as a trigger-ID. The trigger-ID consists of a consecutive 32 bit number of the triggers and a two byte trigger-type information encoding the different trigger types: physics trigger, internal or external lightpulser, pedestal trigger, external trigger input. The trigger-ID is sent to the data-acquisition boards over a dedicated RS-485 bus. The trigger master board also acts as a slow control master for the trigger units, controlling them via an RS-485 bus. For the timing calibration of the DRS4 domino ring sampling chip, the trigger master provides a timing calibration signal on the timemarker line. The trigger master itself is controlled via its 100 Mbit Fast Ethernet interface.

2.5 Ethernet Interface

The whole data-readout in the FACT camera is done via Ethernet. For this purpose two commercial Ethernet switches are integrated into the FACT camera. From these Ethernet switches there are four Gigabit Ethernet links to

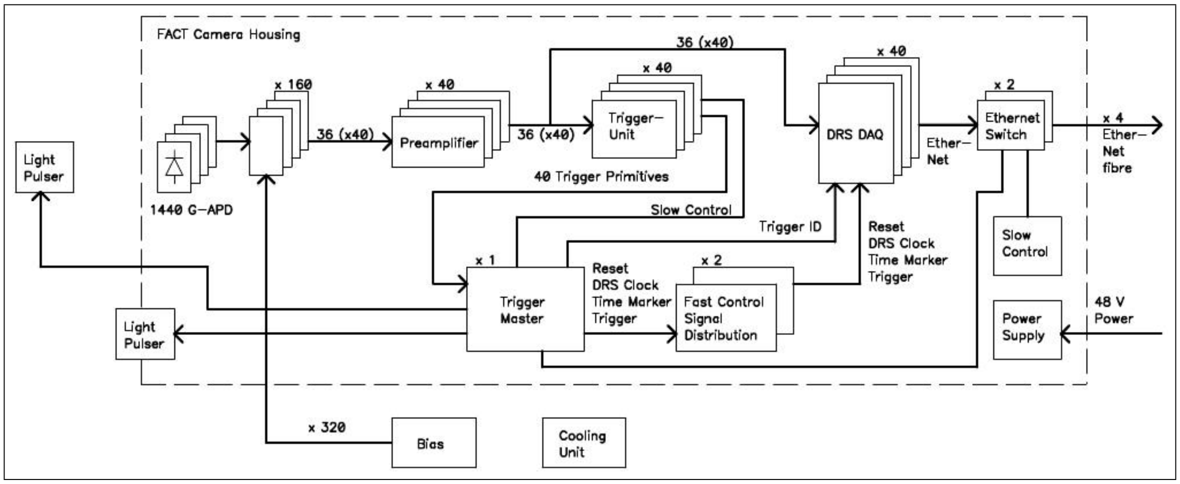

Figure 1: Schematic diagram of the FACT camera electronics

the DAQ computer. These Gigabit links use optical fibres. Measured data rate exceeds 300 MB/s, allowing to operate the camera with up to 1 kHz trigger rate.

2.6 Power- and Bias voltage supply

The FACT camera is powered by an external 48 V DC power supply. A set of power converters inside the FACT camera provides all the necessary low voltage supplies by converting down the 48 V. The total power consumption is on the order of 600 W.

The supply for the G-APD bias voltages is external and comprises 320 channels plus spares. Each trigger patch of nine G-APDs is subdivided into two bias patches of four respectively five G-APDs connected to the same bias channel. The G-APDs were grouped according to their individual breakdown voltages.

3 First results, summary and outlook

The whole trigger- and DAQ electronics has been fully commissioned and installed in the FACT camera as can be seen in figure 2. Various test and performance measurements have been done and are (as per September 2011) still ongoing.

So far, the following performance has been established: The electronic noise of the readout electronics is about 1.8 mV and therefore significantly lower than the signal of a single photoelectron, which is about 10 mV. Therefore, single photoelectron resolution is clearly established. Full-scale reading coresponds to about 200 photoelectrons per pixel. With a readout of the full region of interest (ROI), a read-out rate of 60 - 80 Hz has been reached during laboratory test. Smaller ROIs result in a correspondingly higher maximum trigger rate. In the trigger system, the noise allows a threshold as low as about 20 photoelectrons per trigger patch, corresponding to a mean of about two photoelectrons per pixel. It is forseen to ship the camera to La Palma for integration into the telescope in late September 2011 [8].

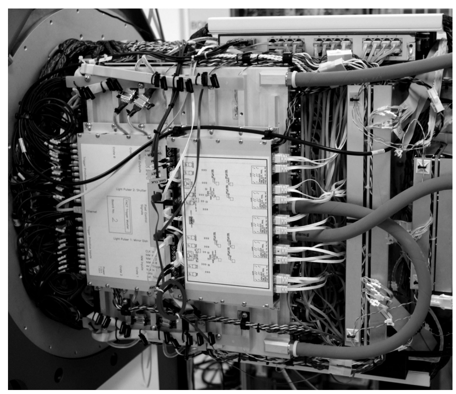

Figure 2: The completed electronics of the FACT camera during laboratory tests.

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